MANUFACTURING METHOD OF A SUPER-JUNCTION SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from application Serial No. JP 2006-285310, filed on Oct. 19, 2006, the contents of which are incorporated herein in their entirety.

BACKGROUND OF THE INVENTION

[0002] A. Field of the Invention

[0003] The present invention relates to a power semiconductor device and, more specifically, to a super-junction (hereinafter may be abbreviated as SJ) MOSFET.

[0004] B. Description of the Related Art

[0005] A MOSFET has been developed which broke through the characteristic limit of conventional silicon MOSFETs by employing, as a drift region, what is called a super-junction structure (hereinafter may be referred to as "p-type/n-type column structure" or "SJ column structure"). A super-junction structure is a collection of column-shaped p-type and n-type regions that are arranged in parallel and in close contact with each other on a high-impurity-concentration (hereinafter referred to as low-resistivity) semiconductor substrate and that extend perpendicularly to its major surface. Mass-production of an SJ-MOSFET initially used a manufacturing method called a multi-stage epitaxial method to realize the super-junction structure. The multi-stage epitaxial method is as follows. An epitaxial layer to serve as a drift layer is grown on a low-resistivity semiconductor substrate in several steps. Patterning and ion implantation are repeated in such a manner that p-type regions and n-type regions having fixed patterns are formed in the epitaxial growth stages of the respective layers, whereby the p-type regions and the n-type regions are connected to each other in the direction perpendicular to the major surface. In this manner, a super-junction structure is formed as a collection of p-type and n-type column-shaped regions that are arranged parallel with each other and extend perpendicularly to the major surface. However, this method requires a long, complex manufacturing process and hence the manufacturing cost and the chip cost are high.

[0006] On the other hand, in recent years, a buried-trench SJ-MOSFET has been developed which can reduce the manufacturing cost. This type of SJ-MOSFET is manufactured in the following manner. A wafer is formed in which an n-type epitaxial layer is grown on a low-resistivity n-type semiconductor substrate. Trenches are formed at prescribed intervals, so as to penetrate through the n-type epitaxial layer and reach the low-resistivity n-type semiconductor substrate, by performing etching from the wafer front side (in some cases, trenches are formed so as not to completely penetrate through the n-type epitaxial layer and hence not to reach the substrate). Then, the trenches are filled in completely by causing p-type epitaxial layers to grow in the respective trenches, whereby a p-type/n-type column structure is formed. The manufacturing process of this method is shorter and simpler than that of the above-described multi-stage epitaxial method, and hence this method may reduce the manufacturing cost.

[0007] In versions of the buried-trench epitaxial method that have been developed to date, MOS gate structures each of which consists of p-type base regions, n-type source regions, a gate oxide film, a channel region, etc of a MOSFET are formed after formation of a p-type/n-type column structure. However, a phenomenon occurs that the impurities in the p-type and n-type columns move by diffusion due to thermal history that is necessary for formation of the MOS gate structures. If the p-type or n-type impurity in each column diffuses into other columns (mutual diffusion), the net doping concentration (i.e., the difference between the p-type doping concentration and the n-type doping concentration) of each column decreases. To compensate for this phenomenon, it is necessary to set the p-type and n-type impurity dopes higher in advance (otherwise the on-resistance becomes high). This increases the absolute values of the variations of the impurity dopes, which leads to a problem that resulting large variations in breakdown voltage lower the breakdown-voltage-related yield. The above problem of mutual diffusion is unavoidable also in the above-described multi-stage epitaxial method which is already in the mass-production stage, and is one of reasons why the breakdown-voltage-related yield of SJ-MOSFETs generally is not very high.

[0008] FIG. **2**A is a schematic sectional view of an SJ column structure for illustration of the above-described impurity mutual diffusion phenomenon. As shown in FIG. **2**A, an SJ column structure which is a collection of p-type regions **3** and n-type regions **2** is formed on low-resistivity n-type semiconductor substrate **1**. The solid line in FIG. **2**B indicates a net doping concentration profile (which is step-like at the p_n junction), taken across the cross section, of a portion indicated by an arrow in FIG. **2**A in the case where the SJ-MOSFET is not subjected to any thermal history after formation of the SJ column structure. The broken line in FIG. **2**B indicates a net doping concentration profile in the case where the SJ column structure is subject to thermal history and in view of reductions in doping concentrations due to mutual diffusion the SJ column structure is given higher impurity concentrations in advance so that the total net doping of p-type region **3** and n-type region **2** are made equivalent to those of the solid-line curve of FIG. **2**A due to mutual impurity diffusion that is caused by the thermal history. Since the total net doping of p-type region **3** and n-type region **2** indicated by the solid line are equivalent to those indicated by the broken line, the breakdown voltage obtained when a reverse bias is applied in the case where the net doping concentration profile is as indicated by the solid line is approximately equal to that in the case where the net doping concentration profile is as indicated by the broken line. (More strictly, because of the difference between the two net doping concentration profiles, different space charge profiles occur when the regions concerned are depleted. Therefore, a small difference exists between the electric field strength profiles and hence a small difference occurs between the breakdown voltages, each of which is the integral of an electric field.)

[0009] Furthermore, the on-resistances of the two cases are approximately identical. In the case of an n-channel MOSFET, the carriers are electrons and hence the resistance of n-type region **2** (one layer) will be calculated below. In the case of the step-like profile indicated by the solid line in FIG. **2**B, the electric conductance σ_1 of the one-layer n-type region **2** is given by

$$\sigma_1 = s_0 D q \rho_{n0} \mu_n / l (\Omega^1) \quad (1)$$